

REMARKS

Claims 1-19 and 22-23 are pending in this application. By this Response, claims 1-7, 9, and 11 are amended, claims 20-21 are canceled, and claims 22-23 are added. Claims 1-7 and 9 are amended for clarification purposes. Claim 1 is further amended to incorporate subject matter from claim 10 which was indicated to be allowable by the Examiner. Claims 22-23 are added to recite a method of providing a pulse width limiting circuit and to recite a pulse width limiting circuit, respectively. Support for these claims may be found at least in the originally filed claims and Figures 3 and 4 of the present specification. Reconsideration of the claims is respectfully requested in view of the above amendments and the following remarks.

I. Telephone Interview

Applicants thank Examiner Almo for the courtesies extended to Applicants' representative during the June 29, 2006 telephone interview. During the telephone interview, the above amendments to the claims to place the application in condition for allowance were discussed. Examiner Almo agreed that, pending an updated search, the above amendments place the application in condition for allowance. The substance of the telephone interview is summarized in the following remarks.

II. Allowable Subject Matter

Applicants thank Examiner Almo for the allowance of claims 10-19. In the Examiner's statement of reasons for allowance of claims 10-19, Examiner stated that the art fails to disclose or suggest "a method for performing a plurality of clock pulse widths limiting in clock pulse comprising disconnecting and resetting individual delay sub-blocks as recited." The feature of disconnecting and resetting individual delay sub-blocks has been added to the other pending independent claim 1, and newly added independent claims 22-23. Accordingly, it is Applicants' understanding that all of the claims should now recite allowable subject matter.

III. Objection to the Drawings

The Office Action objects to the drawings because the reference numerals in the description of Figure 1 do not match the reference numerals set forth in Figure 1. By this Response, the specification is amended to make the description of Figure 1 consistent with the figure. Accordingly, Applicants respectfully request withdrawal of the objections to the drawings.

IV. Claim Objections

The Office Action objects to claims 2, 7 and 11 because of various informalities. With regard to claim 2, the Office Action alleges that the claim should recite that the clock input is coupled "to the drain" rather than "to the source" as the claim currently reads. Applicants respectfully submit that claim 2 is correct as written. As an example, in Figure 4 of the present specification, a circuit arrangement is shown in which the clock input, clock IN 110, is coupled to the source of a PFET, M3P, of clock out hi/lo shuttle 160. This matches the feature recited in claim 2.

The Office Action further alleges that it is improper to refer to a FET as being "positive" or "negative" and that claim 2 should be amended to read a "P-type FET." By this Response, claim 2 is amended to recite a "P-type FET."

The Office Action further objects to claim 7 stating that the claim should recite "a" clock pulse inverter and claim 11 stating that the claim should recite "The method of claim 10..." Appropriate amendments are made to these claims to correct the claims as suggested by the Office Action.

V. Claim Rejections under 35 U.S.C. § 112, Second Paragraph

The Office Action rejects claims 1, 3, 6, 20, and 21 under 35 U.S.C. § 112, second paragraph as being allegedly indefinite for various reasons. This rejection is respectfully traversed.

With regard to claim 1, the Office Action states that it is unclear what is meant by the phrase "conditioned clock signal output" in line 12 of the claim since a clock signal cannot have an output. Applicants respectfully submit that claim 1, line 12 actually recites "a conditioned clock signal output interconnect" (emphasis added). The "interconnect" is a circuit element. Therefore, Applicants respectfully submit that claim 1 is definite as originally presented.

Regarding claim 3, the Office Action alleges that it is unclear what unit comprises the leak detector because in Figure 4, the leak detector is outside the correction block 140. By this Response, claim 3 is amended to recite that the system further comprises a leak detector that is coupled to the clock signal correction block. This is consistent with the depiction of the exemplary embodiment in Figure 4 of the present specification. Therefore, Applicants respectfully submit that claim 3 is not indefinite.

With regard to claim 6, the Office Action alleges that it is unclear which is the conditioned clock pulse because, according to claim 1, the conditioned clock pulse is not between the delay sub-block and the correction block but between the HI/LO shuttle clock and the correction block. Amended claim 6 clearly recites "a node to transmit the conditioned clock pulse between a last delay sub-block of the plurality of delay sub-blocks and the clock signal correction block." Taking Figure 4 as an exemplary embodiment of the present invention, the conditioned clock pulse is the output from delay 4 sub-block 128 which is provided to node A and in turn to the NFET M11N of the correction block 140 and the PFET M7P, which in turn provides the conditioned clock pulse to PFET M4P of the clock out HI/LO shuttle 160. There is nothing unclear in the recited feature of claim 6. To the contrary, the features match those depicted in Figure 4, which again is only one exemplary embodiment of the present invention and is not intended to state or imply any limitation beyond those specifically recited in the claims.

Regarding claims 20 and 21, these claims are canceled by this Response. Thus, the rejection of these claims is rendered moot. For the reasons set forth above, Applicants respectfully submit that the present claims are not indefinite and respectfully request withdrawal of the rejection under 35 U.S.C. § 112, second paragraph.

VI. Claim Rejection under 35 U.S.C. § 103(a)

The Office Action rejects claims 1-9, 20 and 21¹ under 35 U.S.C. § 103(a) as being allegedly unpatentable over Sher (U.S. Patent Application Publication 2001/0011913). As stated above, by this Response, claims 20 and 21 are canceled and claim 1 is amended to incorporate allowable subject matter, i.e. disconnecting and resetting individual delay sub-blocks. Therefore, it is Applicants' understanding that claims 1-9 are now in condition for allowance.

VII. Newly Added Claims 22-23

Claims 22-23 are added to recite a method of providing a pulse width limiting circuit and to recite a pulse width limiting circuit itself. Both of claims 22-23 recite the disconnecting and resetting of individual delay sub-blocks which the Office Action admits to be an allowable feature. Therefore, it is Applicants' understanding that both of claims 22-23 contain allowable subject matter.

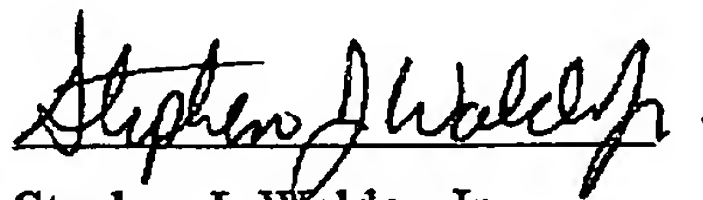
¹ While the statement of the rejection only identifies claim 1, the body of the rejection addresses all of claims 1-9, 20 and 21 and thus, it is assumed that the Examiner intended to reject claims 1-9, 20 and 21 under 35 U.S.C. § 103(a) based on Sher.

VIII. Conclusion

It is respectfully urged that the subject application is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

DATE: June 29, 2006



Stephen J. Walder, Jr.

Reg. No. 41,534

WALDER INTELLECTUAL PROPERTY LAW, P.C.

P.O. Box 832745

Richardson, TX 75083

(214) 722-6419

ATTORNEY FOR APPLICANTS